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INSPECTION

Celero™ PL

Surface and Sub-Surface Defect and Contamination Inspection for Unpatterned Wafer and Epitaxial Layers

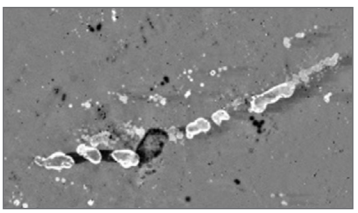
The Celero PL series of tools are designed to fulfill the need for subsurface defect inspection and classification capability for Silicon Carbide (SiC) and Gallium Nitride (GaN) based wafers and compound semiconductor materials. Available in a range of wafer handling options offering the ability to meet both R&D and high-volume production needs while providing best in class throughput and sensitivity at the lowest cost of ownership per pass.

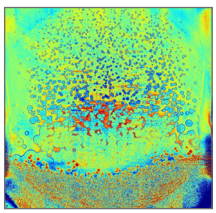
KEY FEATURES AND BENEFITS

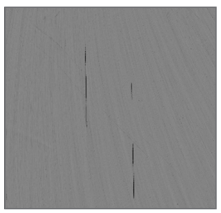
- Wafer sizes: 100-300mm
- Five detection channels
  - Photoluminescence, polarization, slope, BF and DF
- All-surface scan (FS/BS/Edge) and imaging with sub-nanometer sensitivity
- Particle defect (≥90nm PSL) / Surface contamination (≥5Å)
- SiC wafer
  - Particle / Stain / Scratch / Pits / Stacking faults / KOH
- SiC epi
  - Carrots / Triangle / Basal plane dislocation / Pit / Voids
- Substrate-to-epitaxial layer defect mapping (sub-defect mapping)
- Thin (≥100µm) and thick (≤10mm) wafer
- Non-spinning with minimal wafer edge contact
- Multiple handling options
  - Wafer, film frame
- Multiple load options
  - Manual, automated open cassette, EFEM
- Online and offline review capability
- Automated image defect classification

CELERO PL SYSTEM DESCRIPTION

The Celero PL system utilizes a laser-based phase detection and imaging capability that leverages custom optics and image processing algorithms to enable best in class throughput and sensitivity on a broad range of materials and wafer sizes in the rapidly growing compound semiconductor market. Leveraging multiple light sources and sensor channels, the system can detect, measure and image a broad variety of subsurface crystalline defects, associated with bulk wafers and epitaxial layers, surface particles, scratches, pits, surface contamination, stains, point or bulk wafer stress, voids/inclusions, including chips and cracks at the edge of the wafer.


Dark: Top Stain, Bright: Bottom Stain


Post-Clean Water Mark


Surface Scratches

INSPECTION APPLICATIONS

FS / BS / Edge / Subsurface defectivity and contamination

AR/VR/MR materials and structures

Crystalline defectivity in Silicon Carbide (SiC) substrates and epitaxial layers

Crystalline defectivity in Gallium Nitride (GaN) wafers and epitaxial Layers

Thick wafer / Seed wafer surface and sub-surface defectivity

Wafer based microLED / VCSEL / EE laser materials

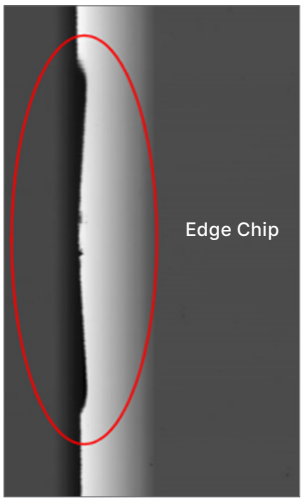
Across wafer and point stress mapping

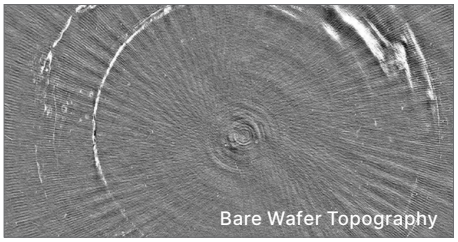
Wafer chuck contamination

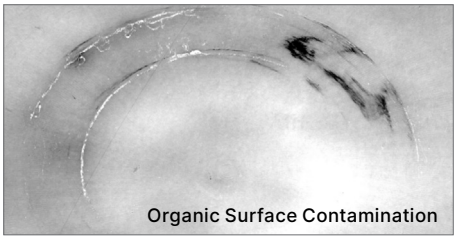
Haze detection and metrology

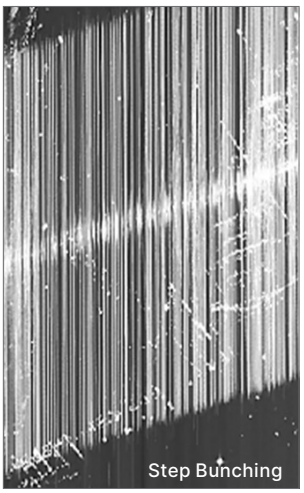
Bow / Warped wafer metrology

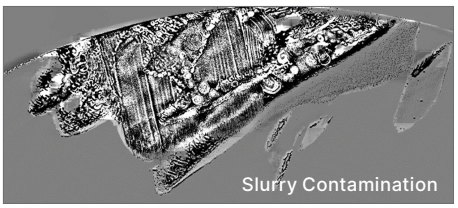
Thinned wafer inspection (including film frame handling)

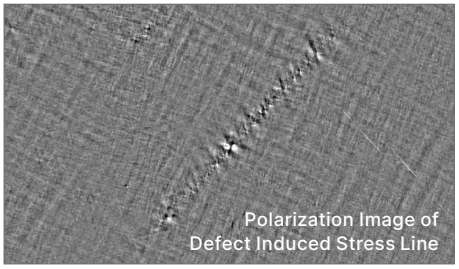


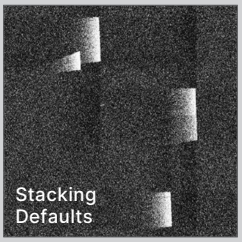


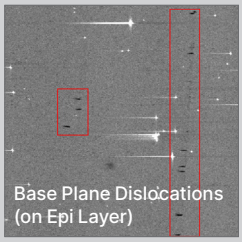


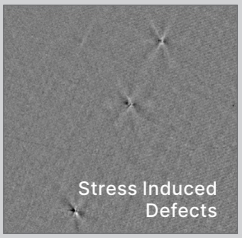


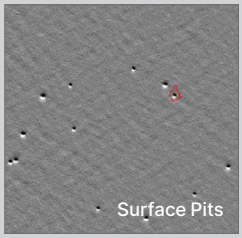


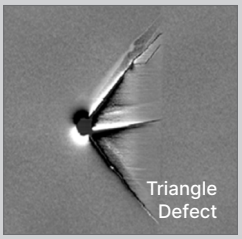


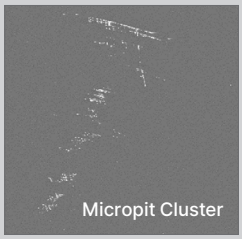


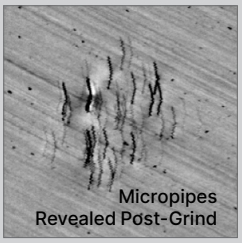












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